CBCS Scheme

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15NT34

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
MOSFETs & Digital Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Define JFET. Discuss the construction of JFET with a neat diagram. **(05 Marks)**

b. Discuss the V-I characteristics of MOSFET. **(05 Marks)**

c. Write a short note on second order effects in MOS. **(06 Marks)**

OR

2 a. With neat diagrams, explain n-well MOS transistor fabrication process. **(10 Marks)**

b. Discuss the types of MOS and draw the input and output characteristics of NMOS transistor. **(06 Marks)**

Module-2

3 a. Explain with neat diagram the CMOS inverter voltage transfer characteristics and mention the regions of operation? **(05 Marks)**

b. Explain the power dissipation equation for CMOS. **(06 Marks)**

c. Write a short note on AOI gate and how it is constructed using CMOS circuits. **(05 Marks)**

OR

4 a. Draw and explain realization of CMOS NOR gate and NAND gate. Verify its functionality. **(08 Marks)**

b. Discuss the delay parameters in CMOS. **(04 Marks)**

c. Write a short note on MOS modeling. **(04 Marks)**

Module-3

5 a. Define sequential circuits. What are the types of sequential circuits? With neat diagram, neither explains the operation of CMOS SR latch using NOR gate. **(10 Marks)**

b. With a neat diagram, explain the operation of D latch. With timing diagram. **(06 Marks)**

OR

6 a. With a neat diagram, explain the operation of JK flipflop. **(07 Marks)**

b. Compare latch with registers. **(04 Marks)**

c. Briefly explain ring oscillator and how in ring oscillator used for on chip clock generation. **(05 Marks)**

Module-4

7 a. Define registers. Explain PISO and SIPO shift registers. **(08 Marks)**

b. Write a note on Johnson counter. **(04 Marks)**

c. Write a note on Ring counter. **(04 Marks)**

OR

8 a. Explain Modulus-8 synchronous up/down counter with a neat diagram. **(06 Marks)**

b. Using JK flip flop, design synchronous counter with the sequence 1, 3, 5, 2, 0, 7. **(10 Marks)**

Module-5

9 a. Explain Mealy and Moore machine models. **(08 Marks)**

b. Design a Mealy state diagram for the sequence 1101. **(08 Marks)**

OR

10 a. Design a Mod-8 synchronous counter using JK flip flop to count number of occurance of an input, i.e. No. of times it is 1. **(12 Marks)**

b. Construct a state table for the following state diagram. **(04 Marks)**

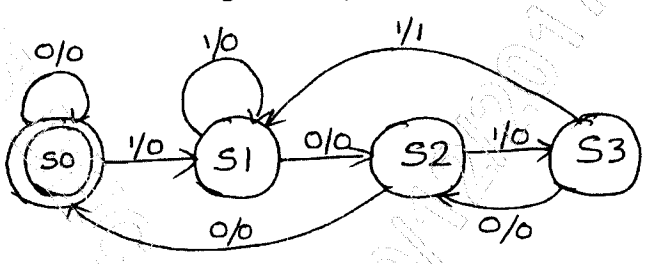

Fig. Q10 (b)

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